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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : THIERRY GRENOT Docket No.: 01-515
Serial No. : 09/914,335 Examiner :
Filed : Art Unit :
PCT No. : PCT/FR00/00311
IFD : February 9, 2000
For : SYSTEM AND METHOD FOR MEASURING
THE TRANSFER DURATIONS AND LOSS
RATES IN HIGH VOLUME TELECOMMUNICATION
NETWORKS

RECEIVED

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INFORMATION DISCLOSURE STATEMENT

Hon. Commissioner of Patents and Trademarks
United States Patent & Trademark Office
Washington, D.C. 20231

Dear Sir:

In compliance with Applicant's continuing duty of disclosure, Applicant hereby submits the prior art documents listed hereinbelow.

- (1) U.S. Patent 5,521,907 for METHOD AND APPARATUS FOR NON-INTRUSIVE MEASUREMENT OF ROUND TRIP DELAY IN COMMUNICATIONS NETWORKS, By Ennis, Jr. et al., Issued May 28, 1996.

This invention relates to measurement of round-trip delay or travel time in a communications network during in-service operation which is accomplished by use of

two probes, situated at respective points of interest along the communication network, and a processor. The probes receive identifiable data patterns normally transmitted over the communications network and generate a time stamp when each pattern arrives at or leaves the respective point. Each probe further generates a pattern identifier based on the data in the pattern and stores the identifier and time stamp as a pair in a buffer internal to each probe. Once the internal buffer contents exceed a predetermined amount of data, the processor receives the data from the buffers and matches pattern identifiers between the buffers to locate the departure and arrival time stamps of each pattern traveling between the probe points. Thereafter, the processor calculates an average of round-trip delay or travel times based on the departure and arrival time stamps of several patterns traveling in both directions between the probe points.

- (2) U.S. Patent 5,535,193 for MULTIPORT ANALYZING WITH TIME STAMP SYNCHRONIZING, By Zhang et al., Issued July 9, 1996.

This invention relates to a plurality of digital transmission network analyzers which are arranged to analyze and compare the appearance of a data packet on the plurality of ports of a network. Each analyzer has its own internal clock for time stamping of data

packets in addition to other internal timing purposes. In order to synchronize the time stamping of the packet as it appears to each analyzer at each different port, the clock outputs of the several analyzers are connected together, and a controlling CPU commands one of the analyzers to supply the master clock to the others. That master analyzer then commands the other analyzers to disable or disconnect their own clocks, thereby all of the analyzers involved in a given test are under timing control of the clock of the master analyzer. Packet headers and time stamps are transmitted between analyzers for comparison, analysis, and reporting to the controlling CPU. This analyzer intercommunication is done over a separate bus that interconnects all of the analyzers and the controlling CPU.

The above documents were cited in a search report issued in a corresponding foreign patent application.

None of the above-referenced patent documents are believed to teach or suggest the present invention.

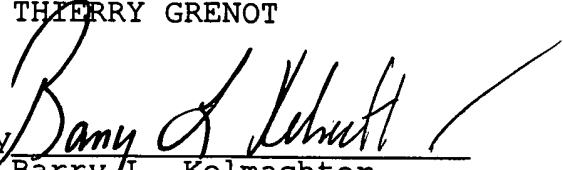
A copy of the patent documents and the search report are enclosed herewith along with a listing of the patent documents on Form PTO-1449.

If any fees are required in connection with this case,
it is respectfully requested that they be charged to Deposit
Account No. 02-0184.

Respectfully submitted,

THIERRY GRENOT

By


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Date: November 5, 2001

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November 5, 2001

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Nicole Motzer

Name and Reg. No. of Attorney



Signature



Date of Signature